What is claimed is:

1. A circuit for outputting a sink current, comprising:

a first current mirror that includes a power transistor and a sense transistor, wherein the power transistor is arranged such that a drain current of the power transistor is substantially greater than a drain current of the sense transistor;

a feedback circuit that is coupled to the first current mirror and arranged such that a drain voltage for the sense transistor is relatively equivalent to a drain voltage for the power transistor;

a follower circuit that is coupled to the first current mirror and arranged such that an output terminal of the follower circuit is coupled to a gate of the power transistor and a gate of the sense transistor, wherein the follower circuit enables the drain current of the power transistor and the drain current of the sense transistor to substantially reach equilibrium in a relatively short period of time if an input signal is asserted; and

a current sinking circuit that is arranged such that the outputted sink current is substantially turned off in a relatively short period of time if the input signal is de-asserted, wherein the current sinking current is coupled to the gate of the power transistor and the gate of the sense transistor.

2. The circuit of Claim 1, wherein the follower circuit enables the outputted sink current to reach a peak value in a relatively short period of time.

3. The circuit of Claim 1, wherein the input signal includes a pulse width modulation signal.

4. The circuit of Claim 3, wherein the pulse width modulation signal operates at a frequency of at least 20 kiloHertz.

5. The circuit of Claim 1, wherein the current sinking circuit includes at least one of a switch and a current sink.

6. The circuit of Claim 1, further comprising a capacitive element that is arranged such that an operation of the capacitive element enables ringing to be substantially reduced.

7. The circuit of Claim 6, wherein the capacitive element is coupled between an input terminal for the follower circuit and a VSS power supply node, wherein an operation of the capacitive

8. The circuit of Claim 1, wherein the feedback circuit includes a second current mirror, and a first transistor and a second transistor that are coupled to the first current mirror, wherein a gate of the first transistor is coupled to a gate of the second transistor.

9. The circuit of Claim 8, wherein an input terminal of the follower circuit is coupled to a drain of the first transistor.

10. The circuit of Claim 8, wherein the feedback circuit includes a third current mirror and a fourth current mirror, wherein the fourth current mirror is arranged to provide a reflected current at a node in response to a reference current, and the third current mirror is arranged to provide another reflected current to the second current mirror in response to the reflected current.

11. The circuit of Claim 10, wherein an input terminal for the follower circuit is coupled to the node.

12. The circuit of Claim 1, wherein the follower circuit includes a source follower.

13. The circuit of Claim 1, wherein the outputted sink current is provided at a drain of the power transistor.

14. The circuit of Claim 1, wherein the outputted sink current is provided at a cathode of a light emitting diode (LED).

15. A circuit for outputting a sink current at a cathode of a light emitting diode (LED), comprising:

a first current mirror that includes a power transistor and another transistor, wherein the power transistor is arranged such that a drain current of the power transistor is substantially greater than a drain current of the other transistor;

a feedback circuit that is coupled to the first current mirror and arranged such that a drain voltage for the other transistor is relatively equivalent to a drain voltage for the power transistor, wherein the feedback circuit includes a second current mirror, and a first transistor and a second transistor that are coupled to the first current mirror, and wherein a gate of the first transistor is coupled to a gate of the second transistor;

a follower circuit that is coupled to the first current mirror and arranged such that an output terminal of the follower circuit is coupled to a gate of the power transistor and a gate of the other transistor, wherein the follower circuit enables the drain current of the power transistor and the drain current of the other transistor to substantially reach equilibrium in a relatively short period of time if a pulse width modulation input signal is asserted; and

a current sinking circuit that is arranged such that the outputted sink current is substantially turned off in a relatively short period of time if the pulse width modulation input signal is de-asserted, wherein the current sinking current is coupled to the gate of the power transistor and the gate of the other transistor.

16. The circuit of Claim 15, wherein the current sinking circuit includes at least one of a switch and a current sink.

17. The circuit of Claim 15, further comprising a capacitive element that is arranged between an input terminal for the follower circuit and a VSS power supply

node, wherein an operation of the capacitive element enables ringing to be substantially reduced.

18. The circuit of Claim 15, wherein an input terminal of the follower circuit is coupled to a drain of the first transistor.

19. The circuit of Claim 15, wherein the feedback circuit includes a third current mirror and a fourth current mirror, wherein the fourth current mirror is arranged to provide a reflected current at a node in response to a reference current, and the third current mirror is arranged to provide another reflected current to the second current mirror in response to the reflected current, and wherein an input terminal for the follower circuit is coupled to the node.

20. The circuit of Claim 15, wherein the follower circuit includes a source follower.

21. A circuit for outputting a sink current, comprising:

a means for mirroring current that includes a power transistor and another transistor, wherein the power transistor is arranged such that a drain current of the power transistor is substantially greater than a drain current of the other transistor;

a means for providing feedback such that a drain voltage for the other transistor is relatively equivalent to a drain voltage for the power transistor;

a means for following a voltage such that the drain current of the power transistor and the drain current of the other transistor to substantially reach equilibrium in a relatively short period of time if an input signal is asserted; and

a means for sinking current such that the outputted sink current is substantially turned off in a relatively short period of time if the input signal is de-asserted, wherein the current sinking current is coupled to the gate of the power transistor and the gate of the other transistor.